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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,251	10/16/2003	Jonathan James DeMent	AUS920030580US1	8990

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EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,251	DEMENT ET AL	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, the recitation "the output" on lines 4, 6, 11, 13 and 14, and "the frequency running clock" on line 5 lacks clear antecedent basis. The same is true for reciting "the input" on line 2 of claim 3, "the core meshing clock" in claims 4 and 8, "the output", "the incrementer" and "the next value" in claim 13, "the delay signal" in claim 14, "the clock frequency" and "the core mesh-clock frequency" in claim 16 and "the clock" in claim 17.

In claim 5, the recitation "the passage" on line 2 lacks clear antecedent basis. It is unclear what the passage of time is and how the storage device can measure the passage of time since the storage device is the means for storing data which cannot perform the measuring function.

In claim 9, it is unclear how the recitation "delaying the voltage level" and "detecting an edge on the voltage level" is read on the preferred embodiment. Insofar as understood, no such

steps are seen on the drawings. Also, it is unclear what the "value" is and where it comes from. The same is true for reciting "the next value" in claim 13.

In claim 10, it is not understood how the increment value can represent a second clock frequency, what the "second clock frequency" is and where it comes from.

In claim 11, it is unclear how the voltage level can be inverted since no means for performing the inverting function is recited in the claim.

In claim 13, it is unclear how the incrementer can be "used" by the memory and where the incrementer comes from.

In claim 14, it is unclear where the "voltage signal" comes from. Also, it is unclear how the step of delaying can "employ" the latches.

In claim 15, it is unclear how the incrementer can "employ" an n-bit adder.

In claim 16, it is unclear what the "clock frequency" and the "core mesh-clock frequency" are and where they come from.

In claim 17, it is unclear where the clock comes from and how the enable signal can be conveyed to the clock since no means for performing the conveying function is recited in the claim. The description of the claimed invention is incomplete because the enable signal is not connected to anything. Thus, the enable signal may not perform the recited function.

The remaining claims are dependent from the above claims and therefore also considered indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9-10 and 16-17 are rejected under 35 USC 102 (b) as being anticipated by Waters (US 5,982,833).

As the best construed, Waters discloses in Figure 5 a circuit comprising:

- a divider or a counter (82) for generating a clock pulse;
- a means (67) for generating a voltage level (CO); and
- a latch (88) for delaying the voltage level (CO);
- an edge detector (84) for detecting edge from the voltage level (CO) to increase a count value to 65 instead of 64 of the counter (82) based on a detected signal (94), see lines 10-15, column 8.

With regard to claim 10, the increment value 65 represented a second clock frequency of 1.538MHZ, see line 13, column 8.

With regard to claims 16-17, the limitation "the clock frequency and the core mesh-clock frequency are not the same frequency" and "an enable signal is conveyed to the clock" is not given a patentable weight because it is not clearly defined in the claims as discussed above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 14 is rejected under 35 USC 103 (a) as being unpatentable over Waters (US 5,982,833).

Waters discloses in Figure 5 a circuit with all of the limitations of the base claim as stated above but does not disclose that the delaying step employs a plurality of latches in series. For example, Waters uses only one latch (88) for delaying the voltage level (CO). However, since the latch circuit is the delay means and cascading more latches circuits would increase the delay time a skilled artisan realizes that, in order to increase the delay time for the voltage level (CO) of Waters, more latch circuits should be used. Thus, employing more latch circuits in the circuit of Waters for the purpose of increasing the delay time is considered to be a matter of a design expedient for an engineer depending upon a particular environment or a particular application in which the circuit of Waters is to be used. Lacking showing of criticality, it would have been obvious to a person having skill in the art at the time the invention was made to employ more latches circuits in the circuit of Waters for the purpose of increasing the delay time that would compensate for delay between signal paths in the circuit.

Allowable Subject Matter

Claims 1-8 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action. The claims are allowed because the prior art of record does not show the first latch, the inverter, the secondary latches, the edge detector, the incrementer and the memory as combined in claim 1.

Claims 11-13 and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. The claims would be allowed because the prior art of record does not show the voltage level is inverted, the value is stored in a memory and the incremeter is an n-bit adder.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DINH T. LE
PRIMARY EXAMINER